

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.

826.1767

APPLICATION NO.

FIRST NAMED INVENTOR

Kwame Osei BOATENG

FILING DATE

November 5, 2001

GROUP ART UNIT

2825

## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

## U.S. PATENT DOCUMENTS

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## OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

VS	AM	K. O. Boateng, H. Takahashi and Y. Takamatsu, "Diagnosing Delay Faults in Combinational Circuits Under the Ambiguous Delay Model," IEICE Transaction on Information and Systems, Vol. E82-D, No. 12, pp. 1563-1571. Dec 1999.
VS	AN	K. O. Boateng, H. Takahashi, and Y. Takamatsu, "Multiple Gate Delay Fault Diagnosis Using Test-Pairs for Marginal Delays," IEIEC Transaction on Information and Systems, Vol. E81-D, No. 7, pp. 706-715. July 1998.
VS	AO	N. Yanagida, H. Takahashi and Y. Takamatsu, "Multiple Fault Diagnosis By Sensitizing Input Pairs," IEEE Design and Test of Computers, Vol. 12, No. 3, pp. 44-52. No date

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6/14/05

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<b>FORM PTO-1449</b> <b>U.S. DEPARTMENT OF COMMERCE</b> <b>PATENT AND TRADEMARK OFFICE</b>  <b>LIST OF REFERENCES CITED BY APPLICANT</b>  <i>(Use several sheets if necessary)</i>	<b>ATTORNEY DOCKET NO.</b> 826.1767	<b>APPLICATION NO.</b> 10542 U.S. PTO 09/985768
	<b>FIRST NAMED INVENTOR</b> Kwame Osei BOATENG	
	<b>FILING DATE</b> November 5, 2001	<b>GROUP ART UNIT</b> 2320
	11/06/01	

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### OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

VS	AM	I. Pomeranz and S. M. Reddy, "On Test Compaction Objectives for Combinational and Sequential Circuits," Proceedings of IEEE International Conference on VLSI Design, pp. 279-284. 1997
VS	AN	S. Kajihara and K. Saluja, "On Test Pattern Compaction Using Random Pattern Fault Simulation," Proceedings of IEEE International Conference on VLSI Design, pp. 464-469. 1997
VS	AO	I. Hamzaoglu and J. H. Patel, "Test Set Compaction Algorithms for Combinational Circuits," Proceedings of ACM International Conference on CAD, pp. 283-289. 1995.

<b>EXAMINER</b> WTHE SIEK	<b>DATE CONSIDERED</b> 6/14/05
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APPLICATION NO.

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Kwame Osei BOATENG

FILING DATE

November 5, 2001

GROUP ART UNIT

1976

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09/985768

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## OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

17	AM	M. S. Hsiao and S. T. Chakradhar, "Partitioning and Reordering Techniques for Static Test Sequence Compaction of Sequential Circuits," Proceedings of the 7 <sup>th</sup> IEEE Asian Test Symposium, pp. 452-457. 1998.
VS	AN	M. S. Hsiao and S. T. Chakradhar, "State Relaxation Based Subsequence Removal for Fast Static Compaction in Sequential Circuits," Proceedings of Design, Automation, and Test in Europe Conf., pp. 557-582. 1998
VS	AO	M. S. Hsiao and E. M. Rudnick and J. H. Patel, "Fast Algorithms For Static Compaction of Sequential Circuit Test Vectors," Proceedings of IEEE VLSI Test Symposium, pp. 188-195. 1999

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